PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yen-Tai Lin, Shih-Jye Shen
Filing Date: 09/13/2002
Docket No.: EMEP0025USA
Serial No.: 10/065,042
Art unit: 2818
Examiner: Le, Thong Quoc

Title: METHOD FOR CONTROLLING A NON-VOLATILE DYNAMIC RANDOM ACCESS MEMORY

To: Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Subject:

1. Information disclosure statement under 37C.F.R.§1.56 and 37C.F.R.§1.97(d).
2. Fee set forth in 37C.F.R.§1.17(p).

Dear Sir/Madam:

This is an Information Disclosure Statement in accordance with the duty to disclose information material to patentability under 37 C.F.R. §1.56. The applicant wishes to make of record the document listed on the accompanying form PTO/SB/08. It is respectfully requested that the examiner initials the cited reference on the form and that it be made of record in the application and that a copy of the initialed

form be sent to the applicant with the next communication from the examiner.

Since the IDS is filed before payment of the issue fee, a petition to request consideration of the information disclosure statement is hereby requested according to 37C.F.R.§1.97(d). The prior art patent contained in the information disclosure statement was cited in communications from the Taiwan Intellectual Property Office on Sept. 05, 2003. The applicant sincerely hopes that the examiner can consider the item contained in the information disclosure statement.

According to the requirement set forth in 37 C.F.R.§1.98 and M.P.E.P. 609 (Rev.1, Feb. 2000), the applicant is submitting a copy of the cited reference (Taiwan Patent No. 395,056) and a concise explanation of the relevance in this application hereinafter.

TP No.395,056 teaches to a non-volatile memory device. Fig.1 is a block diagram illustrating a first cited art non-volatile memory device 100. The non-volatile memory device 100 includes a memory cell array 104. Each memory cell has a cell transistor and a control transistor. Gates of the cell transistors MC11, MC21 are connected to a word line WL1, and gates of the cell transistors MC12, MC22 are connected to another word line WL2. Sources of the cell transistors MC11, MC12, MC21, MC22 are connected to a source line SL. Gates of the control transistors MS11, MS21 are connected to a control line ML1, and gates of the control transistors MS12, MS22 are connected to another control line ML2. A source line decoder 116, a SG decoder 114, a Y decoder 108, and a WL decoder 106 are used for selecting the cell transistors MC11, MC12, MC21,

MC22.

Fig.2 is a magnified circuit diagram illustrating the cited art memory cell array 104 shown in Fig.4. A plurality of signal lines are used for driving control transistors. For instance, a signal line L1 is capable of delivering a driving voltage provided by the SG decoder 114 to a corresponding control line ML1, and a signal line L2 is capable of delivering a driving voltage provided by the SG decoder 114 to a corresponding control line ML2.

Fig.3 and Fig.4 are section views illustrating the signal line mentioned above. Figs.5-18 are diagrams illustrating fabrication of the cited art non-volatile memory device. Fig.19 and Fig.20 are diagrams illustrating operations of the cited art cell transistor.

Fig.21 is a block diagram illustrating a second cited art non-volatile memory device 200. The non-volatile memory device 200 has a DINOR-type memory cell array 204. SG decoders 114, 205, source line decoders 207, 208, and a WL decoder 106 are used for controlling operations of the cell transistors MC1a, MC1b, MC2a, MC2b, MC3a, MC3b, MC4a, MC4b, the control transistors MS1a, MS1b, MS2a, MS2b, MS3a, MS3b, MS4a, MS4b, and select gates SL1, SL2, SL3, SL4. When reading data stored in the cell transistor MC1a, a sense amplifier 128 senses a voltage shift of a bit line BL1 through a column select gate SLG1. That is, a driving current charges a parasitic capacitor of the bit line BL1 when the cell transistor MC1a is selected. Then, the sense amplifier 128 detects the voltage shift to determine the data ("1" or "0") stored by the cell transistor MC1a.

Fig.22 is a diagram illustrating capacitance calculation of a parasitic capacitor of the bit line shown in Fig.1. Fig.23 is a circuit diagram illustrating capacitance of the bit line within the memory cell array 204 shown in Fig.21. If the select gates SG1, SG2 are turned on, local bit lines SBL1, SBL2 are connected to the bit line BL. Therefore, the capacitance of the external bit line is increased. Fig.24 is a diagram illustrating capacitance calculation of a parasitic capacitor of the bit line shown in Fig.21.

Figs.25-29 are timing diagrams illustrating operations of the cited art non-volatile memory device 200. Fig.30 is a diagram illustrating that current is rapidly increased when the drain voltage exceeds a voltage Vx. However, the cited art has the control transistor connected to the cell transistor. Therefore, the control transistor is capable of preventing the rapidly increased current from affecting the programming operation.

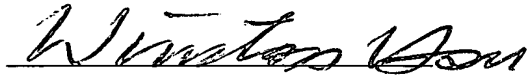
Fig.31 is a diagram illustrating layout of a memory cell shown in Fig.21. Figs.32-33 are diagrams used for illustrating a relationship between an inputted voltage and an effective width Weff. If the effective width Weff is increased, the driving capacity of the transistor is improved. Therefore, the inputted voltage can be accordingly reduced.

Fig.34 is a diagram illustrating a third cited art non-volatile memory device 300. The non-volatile memory device 300 has a NOR-type memory cell array 304. Gates of the cell transistors MC11, MC21 are connected to a word line WL1, and gates of the cell transistors MC12, MC22 are connected

to another word line WL2. Sources of the cell transistors MC11, MC12, MC21, MC22 are connected to a source line SL. A WL decoder 106, an SG decoder 114, and a source line decoder 116 are used for selecting the cell transistors MC11, MC12, MC21, MC22.

Fig.35 is a diagram illustrating voltage conditions for programming the cell transistor that is an n-channel MOS transistor. Fig.36 is a diagram illustrating voltage conditions for programming the cell transistor that is a p-channel MOS transistor. Fig.37 is a circuit diagram illustrating the connection between two cell transistors that are p-channel MOS transistors. Fig.38 is a diagram illustrating voltage conditions associated with the programming operation of the p-channel MOS transistors shown in Fig.37. Figs.39-40 are diagrams illustrating voltage conditions for driving the cell transistors of the non-volatile memory device 300. Fig.41 is a diagram illustrating other voltage conditions for driving the cell transistors of the non-volatile memory device 300, and Fig. 42 is a corresponding timing diagram. The remaining Figs. 43-50 are diagrams illustrating the prior art non-volatile memory device.

Respectfully Submitted,



Date: 4/19/2005

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Approved for use through 10/31/2002. OMB 0651-0031
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/065,042
Filing Date	09/13/2002
First Named Inventor	Yen-Tai Lin
Art Unit	2818
Examiner Name	Le, Thong Quoc
Attorney Docket Number	EMEP002/5USA

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	1	TW 395056	06-21-2000			

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 180.00

Complete if Known	
Application Number	10/065,042
Filing Date	09/13/2002
First Named Inventor	Yen-Tai Lin
Examiner Name	Le, Thong Quoc
Art Unit	2818
Attorney Docket No.	EMEP0025USA

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0801

Deposit Account Name: North America International Patent Office

The Director is authorized to: *(check all that apply)*

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☑ Charge any additional fee(s) or any underpayment of fee(s)

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		x =
Independent Claims		- 3** =		x =
Multiple Dependent				= 0.00

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	180.00
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 180.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Winston Hsu	*Registration No. (Attorney/Agent)*	41,526	*Telephone*	886289237350
Signature	Winston Hsu			*Date*	9/19/2003

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This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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